AMENDMENTS TO THE CLAIMS

1. (Currently amended): A method in a data processing system for preventing said system from crashing when a parity error occurs in a cache that is associated with a processor included in said system and for processing [[a]] said parity error during runtime of said system, the method comprising:

responsive to an occurrence of a parity error in said cache that is associated with said processor, storing a single set of processor information, that indicates an error type, error states, and error status that are stored in said processor as a result of said occurrence of said parity error, in registers in said processor to form stored processor information;

determining whether the parity error is a recoverable parity error using the stored processor information by reading said registers to analyze said stored error type, error states, and error status; and

responsive to the parity error being a recoverable parity error, performing a recovery action.

2. (Currently amended): The method of claim 1, wherein the performing step comprising:

if [[an]] said error type for the parity error is one of a level one data cache error or a level one cache tag error, incrementing an error count associated with the error type and invalidating the level one data cache; and

if the error count associated with the error type is greater than a threshold, disabling the failing portion of the level one data cache or data cache tag.

3. (Currently amended): The method of claim 1, wherein the performing step comprises:

if [[an]] said error type is a translation lookaside buffer error, incrementing a translation lookaside buffer error count and invalidating all entries in a translation lookaside buffer.

4. (Original): The method of claim 3, wherein the performing step further comprises:

if the translation lookaside buffer error count is greater than a threshold, disabling the failing portion of the translation lookaside buffer.

5. (Currently amended): The method of claim 1, wherein the performing step comprises:

if [[an]] said error type is an effective to real address translation error, incrementing [[and]] an error count and invalidating selected entries within a translation lookaside buffer.

6. (Original): The method of claim 5, wherein the selected entries are every fourth entry within the translation lookaside buffer.

7. (Original): The method of claim 5, wherein the performing step further comprises:

if the effective to real address translation error count is greater than a threshold, disabling the failing portion of the effective to real address translation unit.

8. (Original): The method of claim 1, wherein the stored processor information includes at least one error state.

9. (Currently amended): The method of claim 1 further comprising:

if the parity error is a non-recoverable parity error, generating an indication of the non-recoverable interrupt error and storing said indication in said registers.

10-19. (Canceled)

20. (Currently amended): A data processing system comprising:

a bus system;

a communications unit connected to the bus system;

a memory connected to the bus system, wherein the memory includes a set of instructions; and

a processing unit connected to the bus system, wherein the processing unit includes registers for storing a single set of ~~hardware logic to save~~ processor information that indicates an error type, error states, and error status to form stored processor information in response to the detection of a parity error in said cache that is associated with said processor; branch to the machine check interrupt vector, a runtime system firmware executes by the processing unit at the interrupt vector to determine whether the parity error is a recoverable parity error using the stored processor information by reading said registers to analyze said stored error type, error states, and error status; and perform a recovery action in response to the parity error being a recoverable parity error.

21. (Original): The data processing system of claim 20, wherein the bus system is a single bus.

22. (Original): The data processing system of claim 20, wherein the bus system includes a primary bus and a secondary bus.

23. (Original): The data processing system of claim 20, wherein the processing unit includes a plurality of processors.

24. (Original): The data processing system of claim 20, wherein the communications unit is one of a modem and Ethernet adapter.

25-29. (Canceled)

30. (Original): A data processing system for preventing crashing of said system when a parity error occurs in a cache that is associated with a processor included in said system and for processing a parity error, the data processing system comprising:

storing means, responsive to an occurrence of a parity error in said cache that is associated with said processor, for storing a single set of processor information, that

indicates an error type, error states, and error status that are stored in said processor as a result of said occurrence of said parity error, in registers in said processor to form stored processor information;

determining means for determining whether the parity error is a recoverable parity error using the stored processor information by reading said registers to analyze said stored error type, error states, and error status; and

performing means, responsive to the parity error being a recoverable parity error, for performing a recovery action.

31. (Currently amended): The data processing system of claim 30, wherein the performing means comprises:

incrementing means, if [[an]] said error type for the parity error is one of a level one data cache error or a level one cache tag error, for incrementing an error count associated with the error type and invalidating the level one data cache; and

disabling means, if the error count is greater than a threshold, for disabling the failing portion of the level one data cache.

32. (Currently amended): The data processing system of claim 30, wherein the performing means comprises:

means for incrementing a translation lookaside buffer error count and invalidating all entries in a translation lookaside buffer if [[an]] said error type is a translation lookaside buffer error.

33. (Original): The data processing system of claim 32, wherein the performing means further comprises:

means for disabling the failing portion of the translation lookaside buffer if the error count is greater than a threshold.

34. (Currently amended): The data processing system of claim 30, wherein the performing means comprises:

means for incrementing an effective to real address translation error count and invalidating selected entries within a translation lookaside buffer if [[an]] said error type is an effective to real address translation error.

35. (Original): The data processing system of claim 34, wherein the selected entries are every fourth entry within the translation lookaside buffer.

36. (Original): The data processing system of claim 34, wherein the performing means further comprises:

means for disabling the failing portion of the effective to real address translation unit if the error count is greater than a threshold.

37. (Original): The data processing system of claim 30, wherein the stored processor information includes at least one error state.

38. (Currently amended): The data processing system of claim 30 further comprising:

generating means for generating an indication of the non-recoverable interrupt if the parity error is a non-recoverable parity error and storing said indication in said registers.

39-50. (Canceled)

51. (New): A computer program product in a computer readable medium for preventing said system from crashing when a parity error occurs in a cache that is associated with a processor included in said system and for processing said parity error during runtime of said system, the product including the data processing implemented steps of:

responsive to an occurrence of a parity error in said cache that is associated with said processor, instructions for storing a single set of processor information, that indicates an error type, error states, and error status that are stored in said processor as a result of

said occurrence of said parity error, in registers in said processor to form stored processor information;

instructions for determining whether the parity error is a recoverable parity error using the stored processor information by reading said registers to analyze said stored error type, error states, and error status; and

responsive to the parity error being a recoverable parity error, instructions for performing a recovery action.

52. (New): The product of claim 51, wherein the instructions for performing further comprises:

if said error type for the parity error is one of a level one data cache error or a level one cache tag error, instructions for incrementing an error count associated with the error type and invalidating the level one data cache; and

if the error count associated with the error type is greater than a threshold, instructions for disabling the failing portion of the level one data cache or data cache tag.

53. (New): The product of claim 51, wherein the instructions for performing further comprises:

if said error type is a translation lookaside buffer error, instructions for incrementing a translation lookaside buffer error count and invalidating all entries in a translation lookaside buffer.

54. (New): The product of claim 53, wherein the instructions for performing further comprises:

if the translation lookaside buffer error count is greater than a threshold, instructions for disabling the failing portion of the translation lookaside buffer.

55. (New): The product of claim 51, wherein the instructions for performing further comprises:

if said error type is an effective to real address translation error, instructions for incrementing an error count and invalidating selected entries within a translation lookaside buffer.

56. (New): The product of claim 55, wherein the selected entries are every fourth entry within the translation lookaside buffer.

57. (New): The product of claim 55, wherein the instructions for performing further comprises:

if the effective to real address translation error count is greater than a threshold, instructions for disabling the failing portion of the effective to real address translation unit.

58. (New): The product of claim 51, wherein the stored processor information includes at least one error state.

59. (New): The product of claim 51 further comprising:

if the parity error is a non-recoverable parity error, instructions for generating an indication of the non-recoverable interrupt error and instructions for storing said indication in said registers.